DCM Compressor Port Communication

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Outline:

The compressor port (or zero suppression daughter card) is connected to the DCM board via a AMPFH2X50VR 100 pin connector, one for each of the four parallel SHARC DSP's. The main components of the compressor port are the fiber receiver, GLINK, ALTERA 8k FPGA, dual-port memory, ALTERA 10k FPGA, external list memory, and external pedestal memory.

Upon power up, the 8k FPGA is booted from an on-board EPROM (loaded with program GINTER3). The 10k FPGA is booted by sending the program (COMPRESSOR) from the DSP via the serial port into the 8k FPGA and then into the 10k. The 10k FPGA once booted also receives direct communication from the DSP via serial port connection. Through this path, one can write to list memory, pedestal memory or write threshold values (which are contained in the 10k internal memory).

In data taking mode, one can write fake data directly into the dual-port memory or take data into the fiber receiver (at a frequency of 500 MHz per bit with each word packed into 24 bits – 2 bits for CAV and DAV and 16 data bits), then into the GLINK which parallelizes the data, then into the 8k FPGA, then 16-bit wide into the dual-port memory, then out via the 10k FPGA and directly out to the DSP (generally read out with a DMA transfer).

Communications from the DSP to daughter card components is done via the DSP serial port 0. Using DSP output flags FLG0 and FLG1 one communicates various interface states.

Flag State	FLG0	FLG1
Idle State	0	0
Load Command	1	0
Load Serial Data	0	1
Online	1	1

For loading any memory or configuration via serial transfer, first the Load Command state is selected and the serial port register is set (specifying the number of bits, DMA enable, and least or most significant bit first. Using a 22-bit frame one can do the following operations (with the lower bits specifying the starting memory address for the write/read).

Command/ Serial data bits	**0-16**	**17**	**18**	**19**	**20**	**21**
Write/Read List Memory	Address (0-11)	1	0	0	0	R/W
Write/Read Pedestal Memory	Address (0-16)	0	1	0	0	R/W
Write/Read Zero Suppression Table	Address (0-9)	1	1	0	0	R/W
Write Zero Suppression on/off	N/A	0	0	1	0	1

The write (W=1) and read (R=0) for bit 21. After such a command is selected, the flags state for load serial data is set and the data is transferred. For list memory the data passed in 16 bit words and 4 bits (11-14) are used as a label. The label can indicate start of data packet (0xf) and the AMU cell identifier. There is also an indication of the end of data packet set on the 15^{th} bit.

List Memory Label	**Bits (0-10)**	**11**	**12**	**13**	**14**	**15**
Beginning of Data Packet (15)	Address	1	1	1	1	0
No Zero Suppression (6)	Address	0	1	1	0	0
End of Data Packet (6) + bit 15	Address	0	1	1	0	1

Pedestal memory is set in 8-bit words and has no special labels. Threshold values have 12-bit words and no special labels.

There are another set of commands which can be used via the serial link. The following load commands are 18 bits wide.

Command/ Serial data bits	**13**	**14**	**15**	**16**	**17**
Configure	1	1	1	1	1
Load test data, Use test pages	0	1	1	1	1
Load test data, No test pages	1	0	1	1	1
GLINK Online	0	0	1	1	1
Idle Online	1	1	0	1	1

After setting the command for load test data (placing fake data into the dual-port memory), the fake data is input in 18 bit transfers.

Bits	(0:15)	16	17
Entry	Fake data	DAV	CAV

For all DSP Serial data transfer the following information applies:

- 8 MHz maximum frequency
- clock continuously running
- frame ahead of data
- MSB for all operations except (LSB for configure 10k)

DSP Serial Port Write Setup

data type	right justified, zero filled unused MSB bits
serial data endian	Serial data MSB, 10K Configuration LSB
serial word length	depends
data word unpacking	no
internal generated clock	yes
Gated clock	no
Data, frame synch on clock rising edge	falling edge
Transmit Frame Synch requirement	yes
Internal generated TFS	yes
Data Independent TFS	no
Active Low TFS	No
Late TFS	No

DSP Serial Port Read Setup

data type	right justified, zero filled unused MSB bits
serial data endian	Serial data MSB, 10K Configuration LSB
serial word length	depends
data word unpacking	No
internal generated clock	No
Gated clock	No
Data, frame synch on clock rising edge	Rising Edge
Transmit Frame Synch requirement	Yes
Internal generated TFS	No
Data Independent TFS	No
Active Low TFS	No
Late TFS	No

Event packet summary word

Bit	0	1	2	3-4	5
	Event Type	GLINK Error	parity check	spare	DP page #

Bit	6-7	8-11	12-15
	spare	Word Count(0:3)	Event Count(0:3)

Word Count(0:3): Number of Data word (DAV on)
Event Count(0:3): Number CAV (trailer of packet) Word.